Claims:

Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1-22. (cancelled)

23. (currently amended) An integrated circuit fabricated on a semiconductor substrate and having at least two devices, each of the devices having a different effective gate oxide thickness, the circuit comprising:

a first device having a first gate disposed on a first gate dielectric layer, the first gate dielectric layer having a first thickness and a first effective gate ~~dielectric value~~ oxide thickness and disposed on the semiconductor substrate; and

a second device having a second gate disposed on a second gate dielectric layer having the first thickness and the first effective gate ~~dielectric value~~ oxide thickness, the second gate dielectric layer fabricated on ~~a~~ the semiconductor substrate, the second device comprising:

a buried channel implanted below the second gate dielectric layer in a second region of the substrate, the buried channel being doped with a predetermined dopant of a first conductivity type and the second region having a second conductivity type, the buried channel having a peak concentration of the predetermined dopant positioned at a selected level in the second region ~~substrate of a second conductivity type~~ below the gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer when the second channel is biased with respect to the substrate and the buried channel is partially depleted of charge carriers, to increase the effective gate ~~dielectric~~ oxide thickness of the second device,

wherein the level is selected so that the effective gate ~~dielectric~~ oxide thickness of the second device is a predetermined value greater than the first effective gate ~~dielectric value~~ oxide thickness.

24. (previously added) The integrated circuit as recited in claim 23 wherein the insulating gate dielectric layer and the substrate forms an interface and the peak concentration of implanted dopants in the buried channel is located between 400 and 1000 Angstroms below the interface.

25. (previously added) The integrated circuit as recited in claim 23 wherein the device is a MOS capacitor.

26. (currently amended) The integrated circuit as recited in claim 23 wherein the second region of the substrate is a p-type substrate and the buried channel is an n-type buried channel.

27. (currently amended) The integrated circuit as recited in claim 23 wherein the second region of the substrate is ~~a~~ an n-type substrate and the buried channel is an p-type buried channel.

28. (cancelled)

29. (currently amended) The integrated circuit as recited in claim 23 wherein the first device has a threshold voltage implant having the same concentration and conductivity type as the predetermined dopant formed beneath the second gate and is formed in a first region of the substrate of the first conductivity type.

30. (previously added) The integrated circuit as recited in claim 23 wherein the first gate is doped with a first conductivity type impurity and the second gate is doped with a second conductivity type impurity.

31. (previously added) The integrated circuit as recited in claim 23 wherein the first gate is doped with a second conductivity type impurity and the second gate is doped with a first conductivity type impurity.

32. (new) An integrated circuit fabricated on a semiconductor substrate and having at least two devices, each of the devices having a different effective gate oxide thickness, the circuit comprising:

a first device comprising a surface channel MOS device having an insulating gate dielectric of a first thickness; and

a second device comprising a buried channel MOS device having an insulating gate dielectric of the first thickness and a buried channel implanted into the surface region of the substrate beneath the gate, the buried channel comprising channel dopants opposite to that of the substrate dopants such that the substrate portions above the buried channel act as a supplemental gate dielectric layer when the gate is biased with respect to the substrate and the buried channel is partially depleted of charge carriers, to increase an effective gate oxide thickness of the second device to a value greater than an effective gate oxide thickness of the first device.

33. (new) The integrated circuit as recited in claim 32 wherein the first and second devices are MOS capacitors.

34. (new) The integrated circuit as recited in claim 32 wherein the first and second devices are one of MOS capacitors and MOS transistors.